	L #	Hits	Search Text	DBs	Time Stamp
1	L1	16	alignment adj mark and doped adj oxide	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:13
2	L2	2	doped adj oxide near4 etching and alignment adj mark	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:14
3	L3	4464	hydrogen adj reduction	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:14
4	L4	5	silicon adj nitride near4 hydrogen adj reduction	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:14

	L #	Hits	Search Text	DBs	Time Stamp
5	L5	780	(reduce adj hydrogen or reduced adj hydrogen) and (silicon adj nitride or SiN or Si3N4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:15
6	L6	72	electron adj beam and 5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:15
7	L7	30	reduced adj hydrogen same electron adj beam	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:15
8	L8	736	electron adj beam adj treatment	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:15

	L #	Hits	Search Text	DBs	Time Stamp
9	L9	7	electron adj beam adj treatment same (SiN or silicon adj nitride)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:16
10	L10	30626	dehydrogenation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:16
11	L11	707	silicon adj nitride and 10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:16
12	L12	707	silicon adj nitride and 10	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:16

	L #	Hits	Search Text	DBs	Time Stamp
13	L13	86	(e-beam or electron adj beam) and 12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:17
14	L14	2	10 near4 silicon adj nitride	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/08 18:17

US-PAT-NO: 6664172

DOCUMENT-IDENTIFIER: US 6664172 B2

TITLE: Method of forming a MOS transistor with improved threshold voltage stability

---------- KWIC ---------

Claims Text - CLTX (13):

13. A method of making a metal-oxide-semiconductor (MOS) transistor with improved threshold voltage (V.sub.t) stability, the method comprising: providing a semiconductor substrate; forming the gate of at least one transistor on a surface of the semiconductor substrate, the gate comprising a gate oxide layer and a conductive layer; forming a lightly doped drain (LDD) of the transistor; forming a silicon nitride layer Si.sub.3 N.sub.4 layer) on a surface of the gate of the transistor and the semiconductor substrate by performing a low thermal budget process; performing a **dehydrogenation process on the silicon nitride** layer; etching the silicon nitride layer to form a spacer in the periphery of the gate, and forming a source/drain (S/D) of the transistor.